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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated module, comprising:

an external access terminal;

a memory including memory cells for storing code and data;

a microcontroller connected to said external access terminal and to said memory, said microcontroller controlling an access to said memory and a data transfer through said external access terminal during normal operation, said microcontroller controlling a performance of a test sequence for functional testing said memory in a test operation of the module; and

a defect data memory for storing ~~defect data under control of said microcontroller, the defect data~~ addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing.

Claim 2 (original): The integrated module according to claim 1, further comprising a command memory for storing an

externally supplied command sequence and on a basis of the command sequence said microcontroller controls a carrying out of the test sequence.

Claim 3 (original): The integrated module according to claim 1, wherein said defect data memory is part of said microcontroller.

Claim 4 (original): The integrated module according to claim 2, wherein said command memory is part of said microcontroller.

Claim 5 (currently amended): A method for functionally checking a memory of an integrated module, which comprises the steps of:

reading-in a command sequence externally before beginning a test operation, and on a basis of the command sequence a microcontroller controls a carrying out of a test sequence;

executing the command sequence for carrying out the test sequence by the microcontroller; and

storing ~~defect data~~ addresses of memory cells of the memory which have been detected as defective during the functional

testing in a defect data memory under the control of the microcontroller.

Claim 6 (currently amended): The method according to claim 5, which further comprises:

making a jump to a start address in an internal command memory after the command sequence is read-in at the beginning of the test operation;

executing the command sequence under the control of the microcontroller proceeding from the start address; and

storing the ~~defect data~~ addresses of the memory cells of the memory which have been detected as defective during functional testing generated in the defect data memory under the control of the microcontroller; and

reading-out the ~~defect data~~ addresses of the memory cells of the memory which have been detected as defective during functional testing stored in the defect data memory, under the control of the microcontroller, to outside the integrated module for further evaluation.

Claim 7 (new): The integrated module according to claim 1, wherein said defect data memory and said command memory are part of a dual-port RAM.

Claim 8 (new): The integrated module according to claim 1, wherein the microcontroller is embodied as a hard disk controller.